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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,952	02/12/2004	Hayden C. Cranford JR.	RPS920030108US1	7077
47052	7590	08/04/2005		EXAMINER
SAWYER LAW GROUP LLP PO BOX 51418 PALO ALTO, CA 94303				TAN, VIBOL
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/777,952	CRANFORD ET AL.
Examiner	Art Unit	
Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 25 July 2005.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-21 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 20 and 21 is/are allowed.

6) Claim(s) 1-3,6,7,13 and 19 is/are rejected.

7) Claim(s) 4,5,8-12 and 14-18 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 6, 7, 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doblar et al. (U. S. PAT. 6,338,144) in view of Rai (U. S. PAT. 6,529,036).

In claim 1, Doblar et al. teaches all claimed features in Figs. 1-2, a method comprising: buffering a differential clock signal (C_k , $/C_k$) with a single buffer circuit (26a) for a plurality of load circuits (20a-20c); with the exception of teaching the step of configuring the single buffer circuit to adjust to alterations in the number of load circuits receiving the differential clock signal, wherein noise immunity is increased. However, Rai teaches in Fig. 6, a step of configuring the single buffer circuit (104) to adjust to alterations in the number of load circuits (load circuits would be coupled to outputs 228 and 230) receiving the differential clock signal, wherein noise immunity is increased.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Rai with the teachings of Doblar et al. in order to provide a reduced swing clock buffer that allows high and low output levels to remain constant.

In claim 2, Rai further teaches the method of claim 1 wherein buffering further comprises buffering the differential clock signal (CLK, CLKB) with a differential amplifier circuit (202) including a programmable impedance circuit (234, 226) and a programmable current source circuit (200, 204).

In claim 3, Rai further teaches the method of claim 2 wherein configuring the single buffer circuit further comprises adjusting (232) an impedance level of the programmable impedance circuit (234, 226) and adjusting (100, 112) a current source level of the programmable current source circuit (200, 204).

In claim 6, Doblar et al. teaches all claimed features in Figs. 1-2, a circuit comprising: a clock signal source (12) providing a differential clock signal (Ck, /Ck); and a configurable buffer circuit (26a) for receiving the differential clock signal and providing a clock signal output for a plurality of load circuits (20a-20c); with the exception of teaching wherein the configurable buffer circuit achieves a constant bandwidth and voltage level for the clock signal output while adjusting to alterations in the number of load circuits coupled to the configurable buffer circuit, wherein noise immunity is increased. However, Rai teaches all claimed features in Fig. 6 a configurable buffer circuit (104) achieves a constant bandwidth (matched impedance results in constant bandwidth) and voltage level (col. 1, line 47) for the clock signal output while adjusting to alterations in the number of load circuits coupled to the configurable buffer circuit, wherein noise immunity is increased.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Rai with the teachings of Doblar

et al. in order to provide a reduced swing clock buffer that allows high and low output levels to remain constant.

In claim 7, Rai further teaches the circuit of claim 6 wherein the configurable buffer circuit further comprises a differential amplifier circuit (202) including a programmable output impedance circuit (234, 226) and a programmable current source circuit (200, 204).

Claim 13 corresponds to detailed circuitry already discussed similarly with regard to claim 7.

Claim 19 corresponds to detailed circuitry already discussed similarly with regard to claim 3.

3. Claims 4, 5, 8-12 and 14-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 20 and 21 appear to comprise allowable subject matters.

Response to Arguments

5. Applicant's arguments with respect to claims 1, 6 and 13 have been considered but are moot in view of the new ground(s) of rejection.

The new ground of rejection is set forth, as discussed above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



VIBOL TAN
PRIMARY EXAMINER